A microfabricated surface-electrode ion trap in silicon

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The prospect of building a quantum information processor underlies many recent advances ion trap fabrication techniques. Potentially, a quantum computer could be constructed from a large array of interconnected ion traps. We report on a micrometer-scale ion trap, fabricated from bulk silicon using micro-electromechanical systems (MEMS) techniques. The trap geometry is relatively simple in that the electrodes lie in a single plane beneath the ions. In such a trap we confine laser-cooled $^{24}{\rm Mg}^+$ ions approximately 40 $\mu{\rm m}$ above the surface. The fabrication technique and planar electrode geometry together make this approach amenable to scaling up to large trap arrays. In addition we observe that little laser cooling light is scattered by the electrodes.

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Trapped ions are an attractive system for large scale quantum information processing (QIP) [1, 2]. All the building blocks of such a processor are demonstrated in the laboratory, and there is no known fundamental obstacle to scaling up to a large processor. Nevertheless considerable challenges remain, including methods of manipulating large arrays of ion qubits. Some proposed schemes for QIP in ions involve many interconnected ion traps with integrated optics and control electronics [1, 3, 4, 5, 6, 7]. This paper describes a new approach for making trap structures that is relatively straightforward and holds the potential of scaling up.

A straightforward implementation of a linear radiofrequency (RF) ion trap consists of four parallel conducting rods as depicted in Figure 2(a) [8]. With opposite pairs of rods held at RF-ground and RF potential respectively, a ponderomotive potential arises that provides nearly harmonic confinement in the \hat{x} - \hat{y} radial plane, as in a RF quadrupole mass filter. The RF-grounded rods can be segmented (as illustrated) and a static positive potential (for positive ions) is applied to the end segments relative to the inner segments [9]. This defines a trap zone for charged particles in the \hat{z} axial direction. This type of trap has been used in ion QIP work but may be difficult to implement on a large scale. Key trap characteristics for large arrays of qubits include a small ion-electrode spacing, accurately defined smooth electrode surfaces, low RF losses, compatibility with onchip control electronics, a low anomalous heating rate [4, 10, 11, 12], and the possibility of scaling to many trapping zones [7, 13]. No current trap technology meets all these requirements.

Among several RF ion-trap electrode configurations [9, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24], two ap-

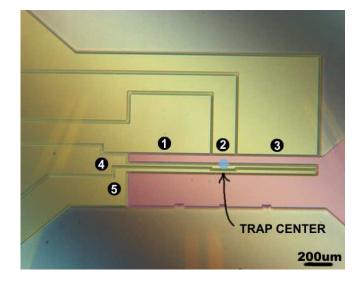


FIG. 1: An image from an optical microscope showing the boron-doped silicon trap viewed normal to the trap surface. False coloring emphasizes the RF electrodes (pink) and control electrodes (yellow). The control electrodes are numbered. Alignment marks on the edge of the outermost RF electrode assist with laser beam alignment. The images in Figs. 5 and 6 were taken in the same view as this figure.

proaches have emerged as possible candidates for scaling to large arrays of traps. One approach uses multilayered structures with large trap depths and open optical access but which are relatively difficulty to fabricate because of the number of layers [16, 18, 19, 20, 21, 22]. Two microfabricated multilayer traps have been demonstrated: in boron-doped silicon [20] and in aluminum-gallium-arsenide [22]. Alternately, single-layer traps, wherein all electrodes lie in a single plane, are more amenable to microfabrication and integration with on-chip control electronics [7, 11], see Figure 2b. Recently this approach was demonstrated for atomic ions in a trap with gold electrodes on a fused silica substrate [23] and with copper electrodes on a GML-1000 printed circuit board [24].

Here we report on the demonstration of a different fab-

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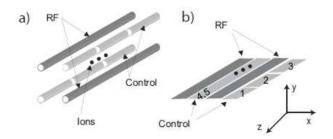


FIG. 2: (a) An idealized geometry for a linear RF Paul trap; (b) A surface-electrode geometry where all electrodes reside in a single plane, with the ions trapped above this plane. [11]

rication technique for surface-electrode traps where the electrodes are lithographically defined from the bulk of a silicon wafer. While the geometry is similar to that in [23], the fabrication method described here has several advantages: the process uses only silicon, so it is compatible with CMOS foundry processes [7]; surfaces exposed to the ion have low surface roughness (< 1 nm RMS); and stray fields from insulators are minimized since the trapping region lies far from the nearest insulating surface, see Figures 1,3, and 4. Using this technology, multizone traps with electrodes 10 μ m wide are practical.

A demonstration trap was fabricated by through-wafer etching of a commercially available boron doped silicon wafer. The electrode pattern was defined by standard photolithography, then etched using deep reactive ion etching (DRIE), a standard MEMS technique also known as the Bosch process [25, 26]. This etch can produce trenches of arbitrary lateral geometry, hundreds of micrometers deep and as small as several micrometers wide while maintaining an etch aspect ratio of 100:1 and low sidewall roughness, see Figure 4. The commercially available silicon is doped with boron as the silicon crystal is grown yielding resistivities of $\rho \simeq 500 \times 10^{-6}$ ohm-cm; no additional metalization is needed in the trap region. For reference, at room temperature $\rho(Au) \simeq 2 \times 10^{-6}$ ohmcm, $\rho(\text{Ti}) \simeq 40 \times 10^{-6}$ ohm-cm and $\rho(\text{W}) \simeq 5 \times 10^{-6}$ ohm-cm [27].

After etching, structural support is provided by anodic bonding of the silicon wafer to a glass substrate [28, 29]. The glass has a gap beneath the trapping region above which the silicon electrodes are cantilevered in vacuum, see Figure 4. This gap is present to keep dielectric surfaces away from the trap region and to reduce the penetration of RF fields into the glass. The glass is a borosilicate (7070) with a loss tangent of 0.060 (1 MHz, 20° C) and a coefficient of thermal expansion (CTE) matched to silicon. For reference, the loss tangent of Pyrex (7740) is 0.500 and that of 99.5% pure alumina is 0.0001 [30].

The anodic bonding is done after thorough cleaning to remove organic contaminants and the native silicon oxide by use of solutions of 8:1 :: $\rm H_2SO_4$: $\rm H_2O_2$ at 90° C and 6:1 :: 40% NH₄F : 49%HF at 25° C, respectively. The

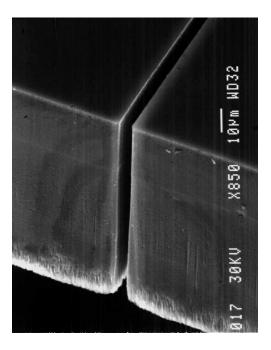


FIG. 3: A SEM image of a 100 μ m thick silicon wafer after through-wafer etching. The dark surface near the top is the wafer's polished top side and was untouched by the etch. This surface was coated with photoresist, then photolithographically patterned to expose bare silicon on the entire lower side and along a 5 μ m wide strip. The wafer was then subjected to etching. In an actual trap the ions would lie above the top surface. The perspective in this image emphasizes (a) the accuracy of the features, (b) the high aspect ratio of the through-wafer etch, and (c) the relative smoothness of the etch sidewalls. The ragged edge at the bottom of the etch is an artifact and can be minimized with proper care.

etch geometry is arranged so that all the electrodes are joined at the periphery until after bonding, whereupon they are separated by a perpendicular cut with a dicing saw [29]. For wiring to external leads, contact pads are made by evaporative deposition of Ti and Cu near the periphery of the chip.

The electrode geometry used here is shown in Figure 1. Five independent static-potential control electrodes are present in this design. The control electrodes define the axial potential curvature and provide sufficient degrees of freedom to properly overlap the static electric field with the RF pseudopotential minimum, that minimizes ion micromotion in both radial directions [11, 23].

Capacitive coupling of the RF and control electrodes due to their close proximity can induce an undesirable RF potential on the latter; this is minimized by coupling the control electrodes to ground through low-pass RC filters mounted on a ceramic chip carrier within the vacuum housing [16].

Ions are created by laser photoionization (PI) of an atomic vapor evolved from a resistively heated ampule containing ²⁴Mg. In some trap designs there is risk of this vapor causing shorts between trap electrodes [23, 24, 31]; the cantilevered geometry avoids this problem as vacuum

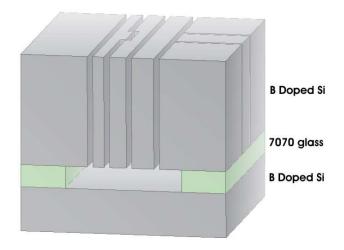


FIG. 4: A schematic view of the trap. A trapped ion would lie above the uppermost layer of silicon. The silicon electrodes overhang the glass frame. In the real structure the glass lies several millimeters away from the trap region.

separates the electrodes in the trapping region. For PI a laser is tuned to the $3s^2$ $^1S_0 \leftrightarrow 3s3p$ 1P_1 electric dipole transition in neutral magnesium at 285 nm [32, 33]. From the 3s3p 1P_1 state, absorption of another photon at 285 nm can excite the electron to the continuum. The PI beam is present in the trap region only during the loading phase.

The ions are Doppler cooled with a 280 nm laser tuned 400 MHz red of the 3s $^2\mathrm{S}_{1/2} \leftrightarrow 3\mathrm{p}\ ^2\mathrm{P}_{1/2}$ electric-dipole transition in $^{24}\mathrm{Mg}^+$. The laser beam propagates parallel to the trap surface, at an angle of 45° with respect to the trap $\hat{z}\text{-axis}$, see Figures 1 and 2b. The radial trap axes lie at approximately 45° with respect to the trap surface. Therefore, the laser has a projection along all three axes, allowing laser cooling along all axes [11].

The cooling and PI beams copropagate. They have a power of 500 μW and 800 μW respectively, measured after they exit the vacuum apparatus. At the trapping region they have a waist of approximately 40 μm and are centered approximately 40 μm above the surface. Ions are detected by observing the ion fluorescence on a CCD camera. The background includes stray light scattered from the cooling laser beam by the apparatus. The signal-to-background for a single ion is higher than 100 : 1 even with a beam intensity 40 times the resonance saturation intensity, limited by noise due to the CCD chip.

Initial trap parameters (RF and control electrode potentials) were determined numerically by the boundary element method. The primary solution constraint is that the micromotion be nulled as discussed above. An ion was first trapped with static potentials of V1 = 0.32, V2 = 0.72, V3 = 0.74, V4 = -0.90 and V5 = 1.00 volts and estimated peak RF potential of $125\ V$ amplitude with respect to DC ground at 87 MHz. For these parameters the expected trap depth is approximately $200\ \text{meV}$,



FIG. 5: A linear crystal of three ions along the trap \hat{z} -axis. With potentials as described in the text the length of the crystal is 13.6 μ m, as expected for the measured axial frequency of 760 kHz.

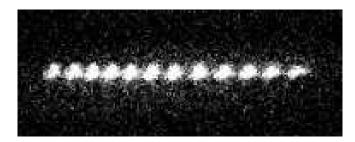


FIG. 6: A linear crystal of 12 ions along trap \hat{z} -axis. The potential on the endcaps is V1=-800 mV and V3=-600 mV. The length of the crystal in the image is 103 μ m.

and the ions are located 40 μm above the surface. Figure 5 shows a linear crystal of three ions trapped using these potentials.

The axial oscillation frequency was measured experimentally by applying oscillating potentials to electrode 1. When resonant with a motional mode of the ions, the motion is excited. We detect this by observing a change in the ion's fluorescence due to Doppler broadening [34]. With the trap parameters listed above, for three ions an axial frequency of 760 kHz was measured. Figure 6 shows a linear crystal of twelve ions achieved by lowering the axial potential on the endcaps to V1 = -800 mV, V2 = 0 mV and V3 = -600 mV. This configuration holds the ions in a linear chain due to a relatively strong axial component of the RF pseudopotential. Single ion lifetimes greater than one hour were observed.

Heating of the ion motion is a concern in all ion traps and is an important consideration in evaluating new fabrication techniques [4, 10, 12, 35] for QIP. Therefore, the next steps in the evaluation of this trap will include characterization of the heating at the quantum level.

It is important to investigate a variety of approaches to ion trap fabrication on the way towards larger QIP processors. Particular attention must be paid to the practicality of scaling to many trapping zones and to material science issues raised by anomalous heating.

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